IN THE CLAIMS:

Add the following new dependent claims:

--65. A storage device employing a flash memory according to claim 63, wherein the storage area includes an array of memory cells that are individually programmable into exactly two states in order to store exactly one bit of data per cell.

B4 66. A storage device employing a flash memory according to claim 63, wherein the storage area includes an array of memory cells that are individually programmable into more than two states in order to store more than one bit of data per cell.--

REMARKS

Two new dependent claims are being added, claim 65 specifying binary (two-state) operation of the individual memory cells, and claim 66 specifying multi-state (more than two states per cell) operation. Although multi-state operation is mentioned in the present application specification, it is more completely discussed in two applications incorporated by reference into the specification at pages 11, 22 and 26. Since the referenced application serial no. 204,175 has issued as patent no. 5,095,344, the patent number is being added by this Amendment. The serial number of the second referenced application is also being added by this Amendment. The status of the second referenced application is that it has become abandoned in favor of a continuation-in-part application which matured into patent no. 5,172,338 and a division thereof into patent no. 5,163,021.

REQUEST FOR DECLARATION OF AN INTERFERENCE

It is respectfully requested that an interference be declared between the present application and patent no. 5,644,539 of Yamagami et al. (hereinafter referred to as the "'539 patent"). Claim 63 of the present application corresponds exactly to claim 9 of the '539 patent. Claim 63 is suggested as the count for the interference, as follows:

Count 1

A storage device employing a flash memory, wherein a storage area of said storage device is divided into a plurality of physical sectors identified by physical addresses, said storage device includes: